YIELD OPTIMIZATION OF A MMIC DISTRIBUTED AMPLIFIER USING PHYSICALLY-BASED DEVICE MODELS

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ABSTRACT

Using a physical model to generate correlated parameters, and response modelling to overcome long response times, even complex circuits can be optimized for maximum yield. In this paper, a MMIC distributed amplifier was simulated and optimized for maximum design yield.

INTRODUCTION

Using conventional optimization strategies available in popular CAD tools, while carrying performance driven optimization, a designer typically optimizes performance only for the nominal values of the circuit parameters, and neglects any statistical fluctuations about the nominal point. For the circuit designed in this fashion, the yield at the nominal point may not result in an acceptable number of "good" circuits once the statistical contribution is considered. Yield optimization is obviously a desirable design procedure, as it simultaneously optimizes both performance and yield. However, it has not gained ready acceptance because of three factors: long simulation times, unavailability of the appropriate statistical data, and unrealistic constraints imposed by the simulation environment. The purpose of this paper is to describe those constraints, and to illustrate how they may be removed.

YIELD OPTIMIZATION

Widely used linear circuit simulators such as SuperCompact [1] and Touchstone [2] allow statistical analysis of arbitrary microwave circuits. Typically a single statistical analysis consists of a frequency sub-loop in which the circuit response is evaluated at every frequency point. This loop is then nested inside an "outcome" loop. In the outcome loop, every statistical variable is randomly perturbed simultaneously with every other statistical variable. The outcome loop is then repeated a number of times; this number is usually referred to as the number of outcomes. The output response of each trial is stored, and may later be plotted as a histogram of values at a particular frequency point. Fig.1 shows a simple flow diagram of the statistical analysis used in SuperCompact.

To illustrate the concepts used in this paper, we chose a two-stage distributed amplifier circuit [3]. The desired response of this circuit is for the linear gain to lie between 10.7 and 11.3 db over a frequency range of 4 to 17 GHz. After performance optimization in SuperCompact, statistical perturbations were added to the circuit parameters. These parameters included the FET small-signal model parameters and the sheet resistivity of the material used to construct the termination resistors. The magnitudes of the perturbations were chosen from typically quoted values for commercial foundries. The active device parameter variations typically dominate other uncertainaties in the circuit. Using Monte Carlo analysis, the yield was estimated to be 74.5%. The yield window is often defined differently from the desired response window that might be used for performance optimization. Here, only circuits that had gain between 9.8 dB and 11.7 dB in the frequency range of 4 to 17 Ghz were accepted. The simulation time to perform this analysis over frequency with 200 trials was 1991 CPU seconds on a MicroVax 3500. The circuit can also be optimized for maximum yield. To achieve this in most linear simulators, the statistical analysis is nested inside an additional loop that performs optimization. This loop calculates the yield and perturbs the optimization variables to determine the effect of that variable on overall yield. From the individual perturbations, an error vector can be found and an optimum search direction calculated. A number of iterations of the optimization loop is then performed until the process converges to a yield maximum. If a

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simulation at a single frequency point takes time Ts, and the number of optimization iterations is No, and if there are Np optimization variables, Ns statistical outcomes (trials), and Nf frequency points, this procedure takes time

$$No * Ns * Np * Nf * Ts,$$

which for large circuits is obviously very large. In the case of the distributed amplifier example above, for 200 statistical outcomes, optimization of the yield took 3488 CPU seconds using SuperCompact on the MicroVax 3500, and the simulated yield improved to 96%. Further improvements in the design yield would require modifications to the circuit topology. This is a fairly lengthy procedure, although not an impractically long time for a relatively complex circuit. However, two problems diminish the confidence the designer has in the results. The first is that the statistical fluctuations are assumed independent. This is an unrealistic assumption especially for active devices. The second problem is that of obtaining data. None of the major FET suppliers provide meaningful (useable) statistical data about their devices, even measured data. Furthermore, even if a designer were to obtain a large sample of devices and MMIC test structures and characterize them, the sheer volume of measured data would be difficult to incorporate into most circuit designs. This could be partially overcome by providing simple, compact representations of this data in the form of the mean and standard deviations, but even this is not enough, because the data is correlated, and the correlation coefficients must also be extracted. The following section addresses solutions to the problems we have identified above.

IMPROVEMENTS TO YIELD OPTIMIZATION ALGORITHMS

Distributions.

One way to overcome the restrictions on using meaningful statistical data is to allow the user to define his own statistical distributions. This can be achieved with a user-defined statistical distribution feature [1]. For instance, if a user is building a filter from discrete components, and requires accuracy in a particular value of inductor, it is possible he will pre-screen those components from a given normally distributed lot. The centrally located values will then be depleted from the lot, leaving the remainder with a non-normal distribution. Using this feature, and using labels to tie together the statistical variables, non-correlated distributions can be handled. However, this feature requires a high degree of knowledge on the part of the user and it is unlikely most designers would go through the effort of transforming their data in order to achieve this. Recently therefore, we introduced correlated parameters, which can be either generated internally or directly from the circuit file description.

Correlations.

The linear correlation relationship between n statistical variables can be represented by an nxn correlation matrix, which is a positive semi-definite symmetrical matrix with unit diagonal elements. The off-diagonal element Cij of correlation matrix is just the linear correlation coefficient between ith and jth statistical variables. Taken from the circuit file, the correlation matrix is decomposed to its LDL decomposition form, which is the product of three matrices: a lower triangular matrix L, a diagonal matrix D, and the transposed matrix of L. This can be used to transfer n normal independently distributed variables to n normal correlated variables with desired correlated coefficients.

Response Modeling.

In order to speed up yield optimization, we implemented a modified quadratic response model [4-6]. This model estimates the circuit performance as a function of the perturbed variables by analytically fitting to a series of simulations. Since the same model is used to evaluate the error functions for both different outcomes and for different optimized parameters in different iterations, the number of complete simulations is reduced from No*Ns*Np to (1+2*Ntp), as the model is used to generate consequent circuit outcomes, once correctly built. Here Ntp is the total number of parameters, i.e. the sum of the number of statistical variables and the number of non-toleranced optimized parameters, so has the same order of magnitude as Np, the number of optimized parameters. With the same number of outcomes, the difference in yield estimated by the model and calculated by exact simulation is less than a few percent. Since the model can be built from a series of complete simulations just once, and reused for the Monte-Carlo trials, it offers a practical way to speed up circuit simulation time.

Device Modeling.
TEFLON [7] is a physical FET model for which the user enters the physical characteristics of a FET, such as the doping density, gate width and length, and material properties. Using this model, independent statistical parameters associated with the fabrication process can be transformed into corresponding statistical distributions for the electrical parameters through the process model. For this example, we made the assumption that the peak doping density in the FET channels has a normal distribution. We also made the assumption that all other process variations could be ignored to first order. Based upon a measured Gaussian distribution of the doping density with standard deviation of 2.77%, forty device simulations were performed using Microwave Harmonica, to determine an equivalent small-signal circuit. This method avoids the problems associated with obtaining statistical data directly from the measurements. Using measured S-parameters, measurement errors and deembedding errors are included in the S-parameter data; these can substantially skew the statistical distribution. The remaining major source of error in using either measured or simulated S-parameter sets is in determining the small-signal equivalent circuit, as residual errors remain as a result of the imperfect fit between the data and the small-signal model used. This is unavoidable when using any large-signal representation of a device. However, the fitting errors were consistently small for all the S-parameter sets fitted, and their effects are neglected when calculating correlation coefficient. The standard deviation and correlation coefficients between each of these elements (for the assumed fluctuation in doping density) are given in Table 1. The major observation to make is that, a variation in a single process parameter can result in correlated, statistical fluctuations in the equivalent circuit model. To illustrate this, Figure 4 shows a crossplot of Cgs and Gds, which have a correlation coefficient of .989. This correlation information was supplied to the simulator in the form of a correlation matrix. Note that the nominal values of the model parameters we used were those originally measured and extracted by the foundry using conventional methods, and on which the design was based. Not all of the process parameters were available for input to the device simulator and especially the device parasitics had to be added afterwards. We used only the normalized distributions and the correlations as they were estimated from multiple device simulations using TEFLON.

SIMULATON RESULTS

The two-stage distributed amplifier described earlier was again subjected to yield analysis, but this time with the relevant statistical parameters having the correlations described in Table 1. The resultant yield prediction was 70.5% as opposed to 74.5% obtained with independent distributions using the same number of outcomes. The circuit was then optimized for yield, subject to the same criteria as above. This time, six of the twelve statistical parameters were correlated with each other; the remaining six were passive elements whose values were independent of the doping density. The final yield estimate after the optimization was 92%, which took 1501 seconds on the MicroVax 3500. This final yield estimate was then tested using "exact" Monte Carlo yield analysis without response modeling, which gave a figure of 91% as an exact yield estimate. Yield optimization of the same circuit using exact Monte Carlo analysis would have required approximately 1.5e5 seconds.

DISCUSSION

As suspected, when yield analysis of a circuit is performed with and without considering the correlations between circuit parameters, a significant difference is observed resulted in an optimistic estimate of the yield. In general the sign of the change is related to the topology, the type, and the amount of correlation that exists, so that any meaningful generalizations are not possible. By way of illustration, Fig.3 shows two possible response windows mapped into parameter space; on the first, the correlations between the two circuit parameters selected as axes fall in such a way as to maximize the number of outcomes falling within the desired mapping of the response window; on the second, they minimize the yield. It is possible to account for any other source of disturbance by the approach we have taken. When this is done it is very likely that the spreads in the statistics will increase. Even though we have modelled the disturbances in our example with normal distributions for the sake of simplicity, this is not a restriction. In fact, there is some evidence that FET parameter statistics are non-Gaussian. In such a case one may resort to user-defined table input for the statistics, and avoid lengthy transformations and normalizations of the initial statistical data. However, experience indicates that to first order, the type of the distribution has very little effect on the circuit sensitivities compared with the spread of the distribution. It is of some interest to see how the nominal values of optimizable parameters changed as a result of de-sensitization of the amplifier gain to peak doping density variations. The nominal values of some of the optimized transmission line lengths did not need to vary more than about 5% to accomplish more than a 28% increase in the overall yield. In such a case, this is fortunate since it implies that slight rework of the layout can result in large improvements in productivity. It is also obvious that a circuit of this complexity can not routinely be optimized for yield without the speed improvements attained by response modeling.

CONCLUSION

We have shown and illustrated an approach that should enable better cicuit designs to be produced. Firstly, fitting the modelled circuit response to a simplified model that is a function only of the statistically perturbed circuit parameters enables enormous speed increases with little observed degradation in accuracy. Secondly, modelling devices at the process level allows meaningful data about the statistical parameters of devices to be deembedded. Finally, improvements to the simulators, some of which now accept correlated and user-defined statistical data entry, allow realistic yield determination during the design phase.

TABLE 1

	G	RI	CGS	CDG	CDS	GDS
G	1					
RI	-.57	1				
CGS	.76	-.9	1			
CDG	.7	-.91	.9	1		
CDS	-.13	-.2	-.12	.08	1	
GDS	.77	-.92	.99	.93	-.005	1

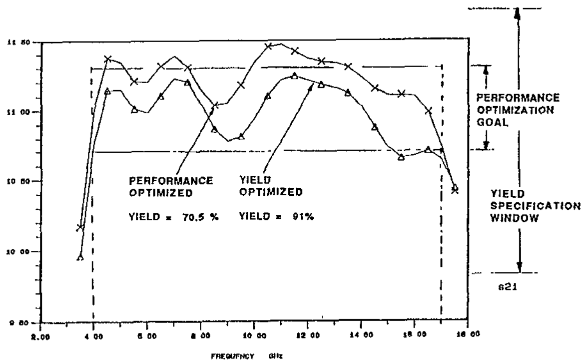

Fig. 4 - Nominal amplifier gain before and after design centering.

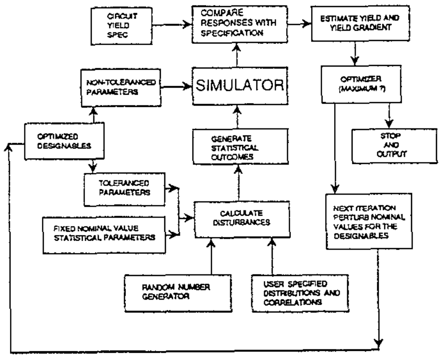

Fig 1 - Flow diagram of statistical analysis and optimization.

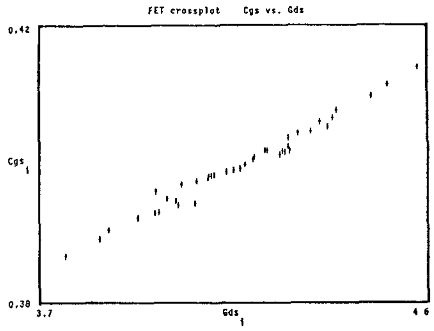

Fig 2 - Crossplot of the two FET model parameters.

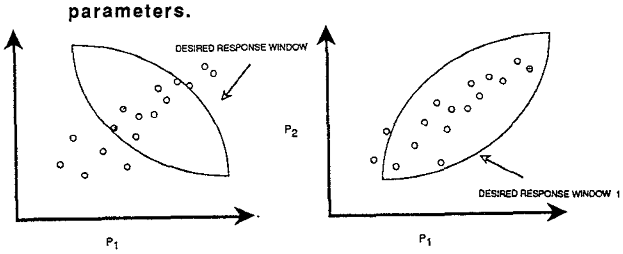

Fig 3 - Two possible response windows for the same correlation between two parameters.

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